

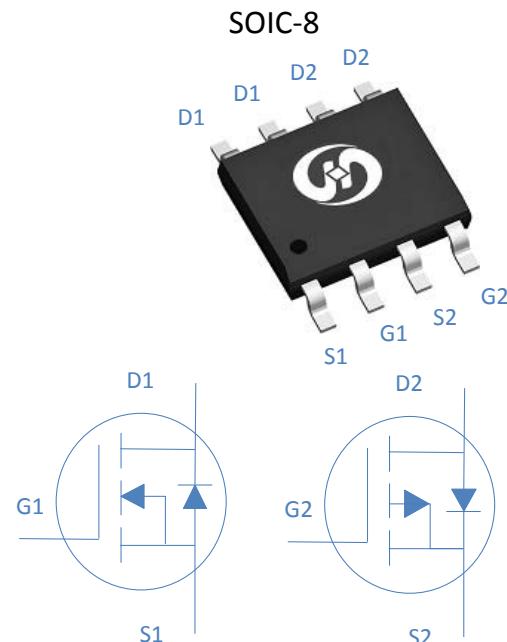
30V Dual N+P Channel Power MOSFET
Feature

- ◊ High Speed Power Switching, Logic Level
- ◊ Enhanced Avalanche Ruggedness
- ◊ Lead Free, Halogen Free

	N-CH	P-CH	
V_{DS}	30	-30	V
$R_{DS(on),max}$	21	35	$m\Omega$
I_D (Silicon Limited)	7.5	-6	A

Application

- ◊ Hard Switching and High Speed Circuit
- ◊ BLDC motor



Part Number	Package	Marking
HTS210C03	SO8	TS210C03

Absolute Maximum Ratings at $T_j=25^\circ C$ (unless otherwise specified)

Parameter	Symbol	Conditions	N-CH	P-CH	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_A=25^\circ C$	7.5	-6	A
		$T_A=100^\circ C$	5.5	-5	
Drain to Source Voltage	V_{DS}	-	30	-30	V
Gate to Source Voltage	V_{GS}	-		± 20	V
Pulsed Drain Current	I_{DM}	-	30	-24	A
Power Dissipation	P_D	$T_A=25^\circ C$		2	W
Operating and Storage Temperature	T_J, T_{stg}	-		-55 to 150	$^\circ C$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$
Thermal Resistance Junction-Case	$R_{\theta JC}$	25	$^\circ C/W$

N-Channel Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_D=250\mu\text{A}$	30	-	-	V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_D=250\mu\text{A}$	1.0	1.5	3.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=24\text{V}, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=20\text{V}, T_j=125^\circ\text{C}$	-	-	25	
Gate to Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Drain to Source on Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=10\text{V}, I_D=7.5\text{A}$	-	17	21	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_D=5.5\text{A}$	-	25	30	
Transconductance	g_{fs}	$V_{\text{DS}}=5\text{V}, I_D=7.5\text{A}$	-	16	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=15\text{V}, f=1\text{MHz}$	-	520	-	pF
Output Capacitance	C_{oss}		-	88	-	
Reverse Transfer Capacitance	C_{rss}		-	62	-	
Total Gate Charge	$Q_g(10\text{V})$	$V_{\text{DD}}=15\text{V}, I_D=7.5\text{A}, V_{\text{GS}}=10\text{V}$	-	11.5	-	nC
Total Gate Charge	$Q_g(4.5\text{V})$		-	5.0	-	
Gate to Source Charge	Q_{gs}		-	1.6	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	2.8	-	
Turn on Delay Time	$t_{\text{d}(\text{on})}$		-	11	-	
Rise time	t_r	$V_{\text{DD}}=15\text{V}, I_D=1\text{A}, V_{\text{GS}}=10\text{V}, R_G=6\Omega,$	-	16	-	ns
Turn off Delay Time	$t_{\text{d}(\text{off})}$		-	36	-	
Fall Time	t_f		-	20	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{\text{GS}}=0\text{V}, I_F=2.3\text{A}$	-		1.3	V
Reverse Recovery Time	t_{rr}	$I_F=2.3\text{A}, dI_F/dt=100\text{A}/\mu\text{s}$	-	50	-	ns
Reverse Recovery Charge	Q_{rr}		-	2	-	nC

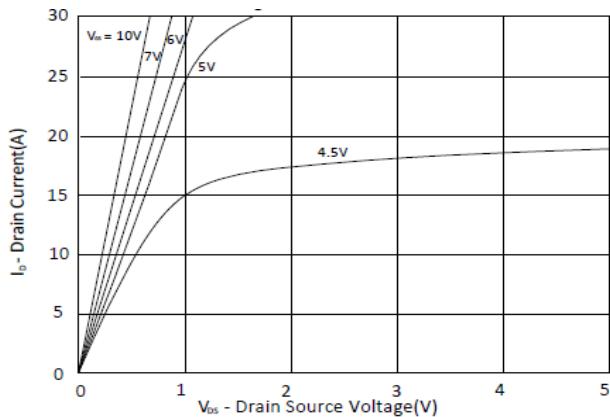
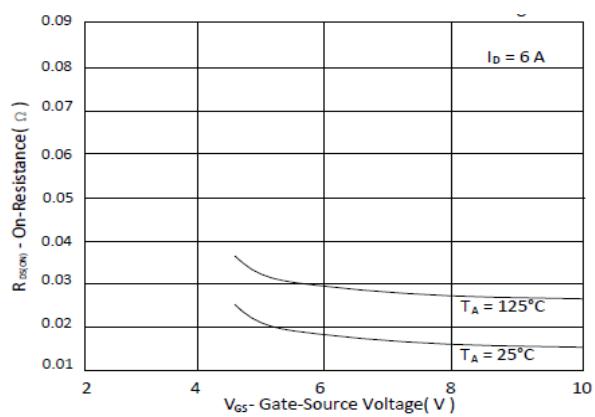
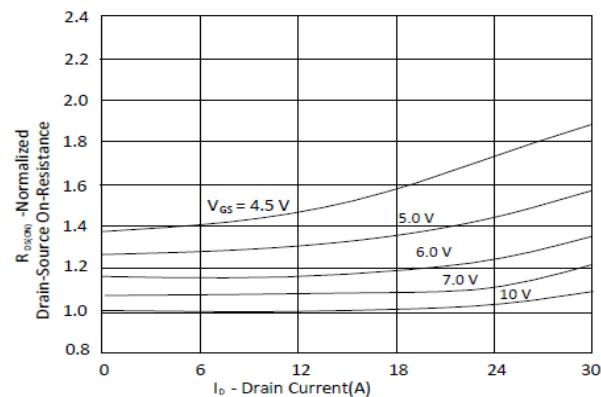
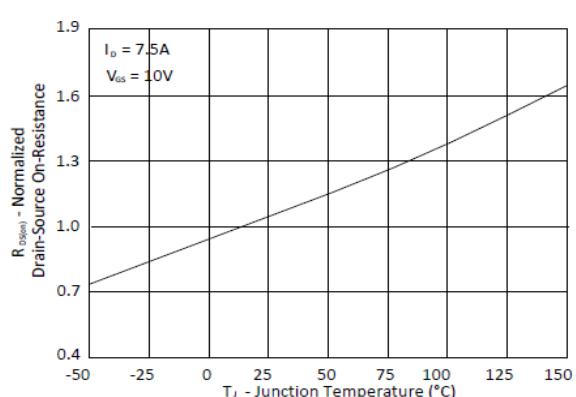
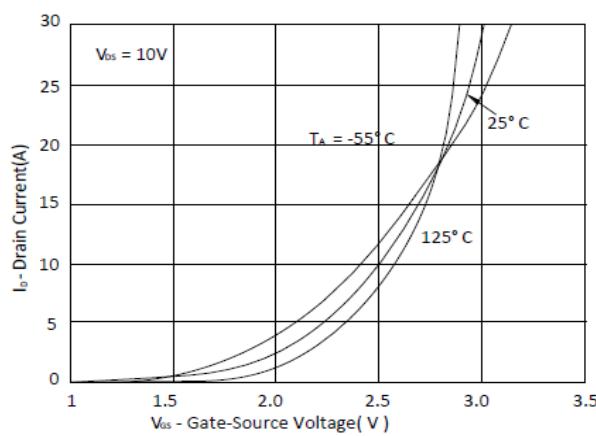
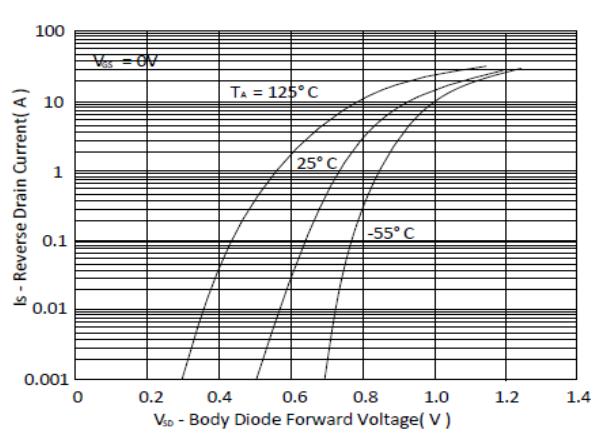
Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. On-Resistance vs. Drain Current and Gate Voltage

Figure 4. Normalized On-Resistance vs. Junction Temperature

Figure 5. Typical Transfer Characteristics

Figure 6. Typical Source-Drain Diode Forward Voltage


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

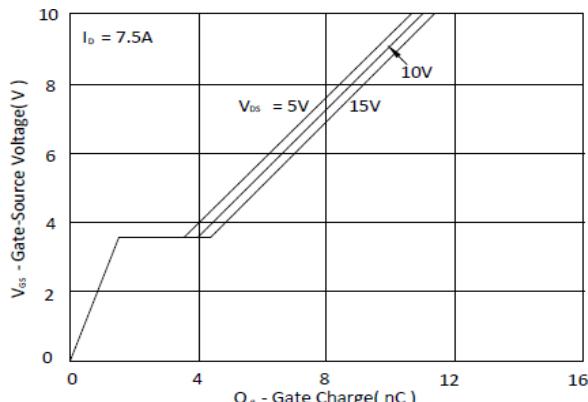


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

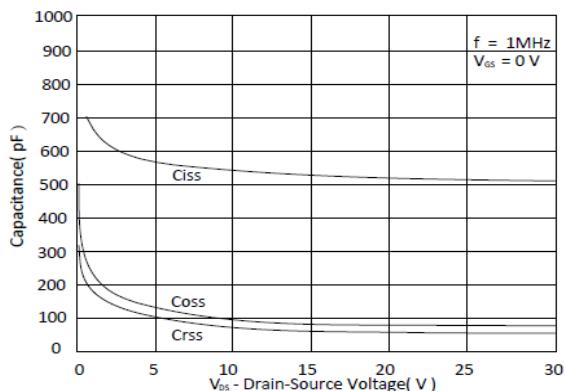


Figure 9. Maximum Safe Operating Area

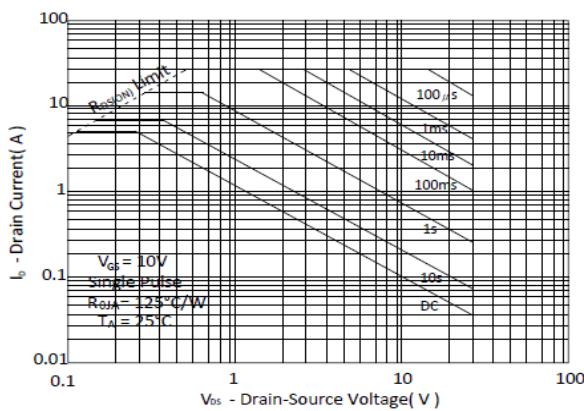


Figure 10. Single Pulse Maximum Power Dissipation

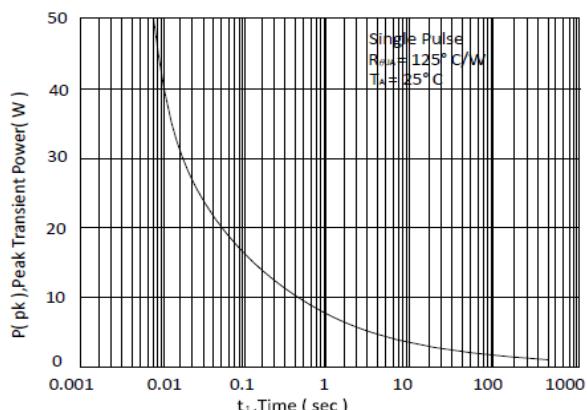
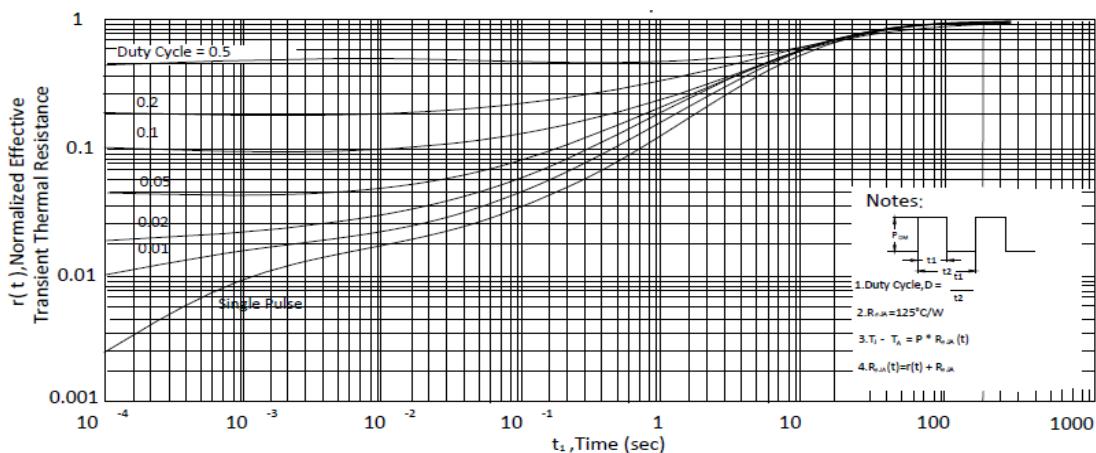


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





P-Channel Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_D=-250\mu\text{A}$	-30	-	-	V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_D=-250\mu\text{A}$	-1.0	-1.5	-3.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-24\text{V}, T_j=25^\circ\text{C}$	-	-	-1	μA
		$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-20\text{V}, T_j=125^\circ\text{C}$	-	-	-25	
Gate to Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Drain to Source on Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=-10\text{V}, I_D=-6\text{A}$	-	30	35	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_D=-5\text{A}$	-	50	60	
Transconductance	g_{fs}	$V_{\text{DS}}=-5\text{V}, I_D=-6\text{A}$	-	12	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-15\text{V}, f=1\text{MHz}$	-	910	-	pF
Output Capacitance	C_{oss}		-	143	-	
Reverse Transfer Capacitance	C_{rss}		-	108	-	
Total Gate Charge	$Q_g (10\text{V})$	$V_{\text{DD}}=-15\text{V}, I_D=-6\text{A}, V_{\text{GS}}=-10\text{V}$	-	13.3	-	nC
Total Gate Charge	$Q_g (4.5\text{V})$		-	7.0	-	
Gate to Source Charge	Q_{gs}		-	2.1	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	3.2	-	
Turn on Delay Time	$t_{\text{d}(\text{on})}$		-	12	-	
Rise time	t_r	$V_{\text{DD}}=-15\text{V}, I_D=-1\text{A}, V_{\text{GS}}=-10\text{V}, R_G=6\Omega$	-	18	-	ns
Turn off Delay Time	$t_{\text{d}(\text{off})}$		-	38	-	
Fall Time	t_f		-	22	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{\text{GS}}=0\text{V}, I_F=-4\text{A}$	-		-1.3	V
Reverse Recovery Time	t_{rr}	$I_F=2.3\text{A}, dI_F/dt=100\text{A}/\mu\text{s}$	-	55	-	ns
Reverse Recovery Charge	Q_{rr}		-	2.2	-	nC

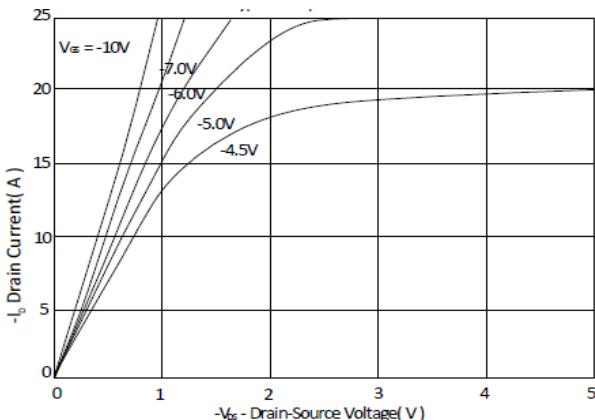
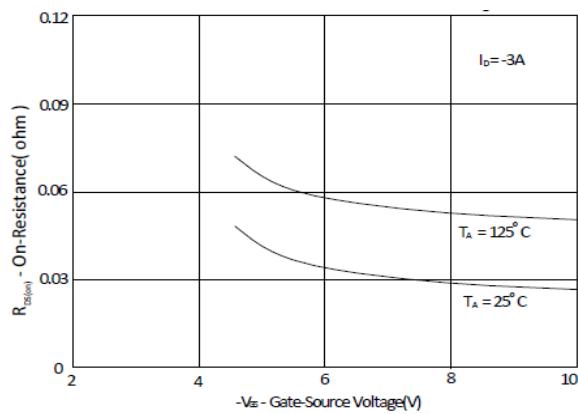
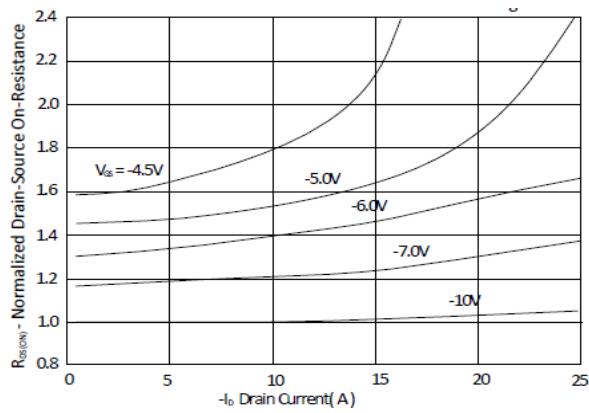
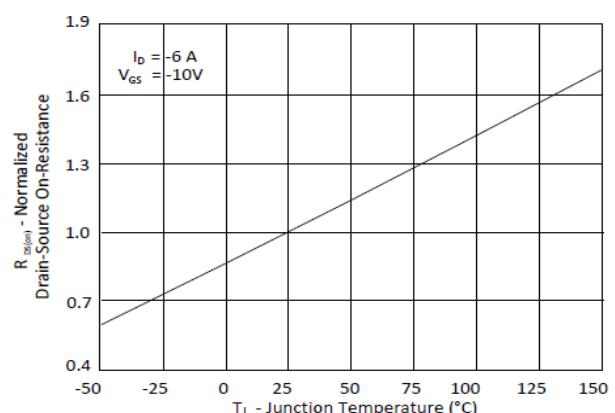
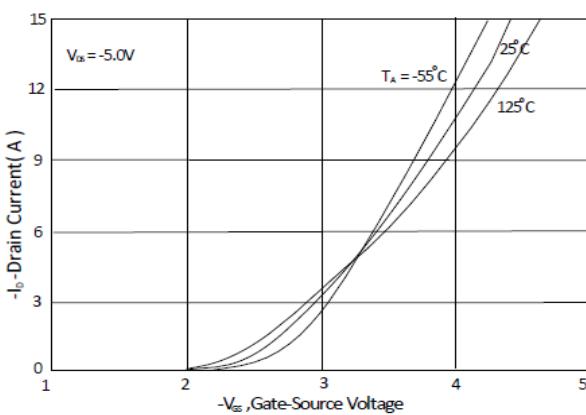
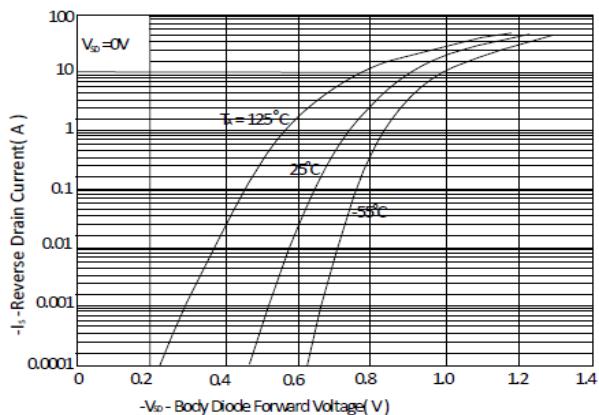
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Figure 2. On-Resistance vs. Gate-Source Voltage

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Figure 6. Typical Source-Drain Diode Forward Voltage


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

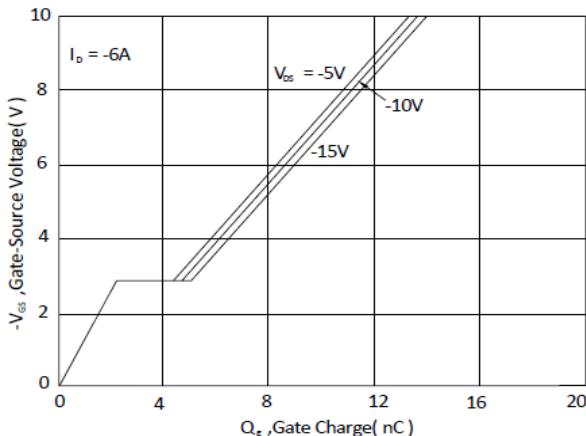


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

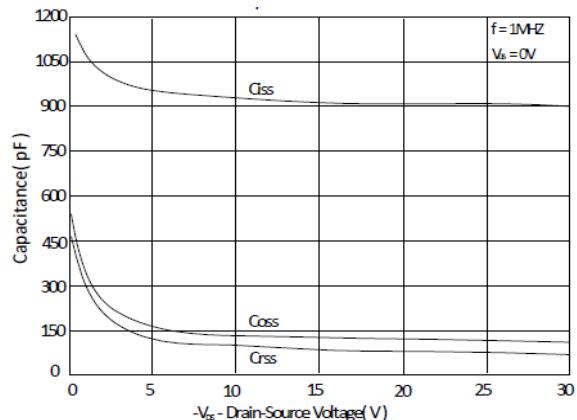


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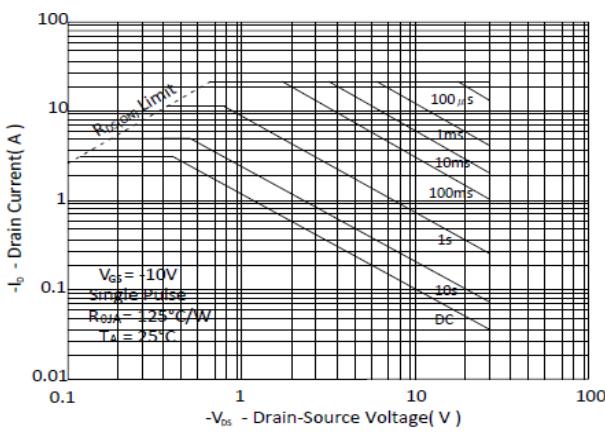


Figure 10. Single Pulse Maximum Power Dissipation

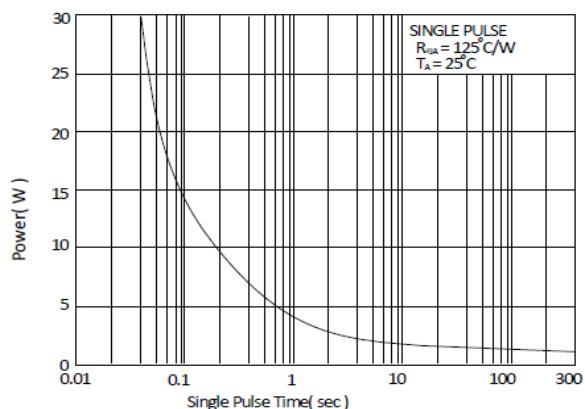
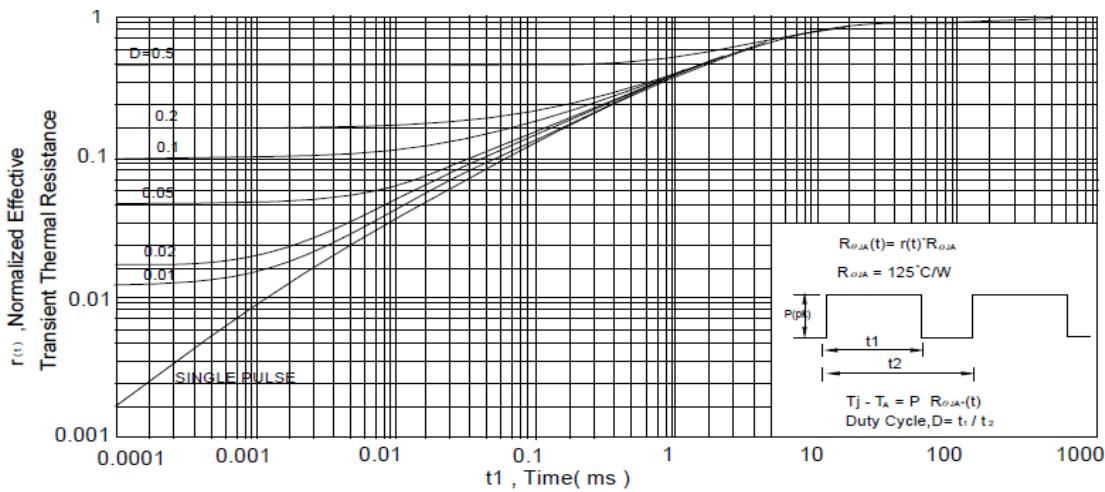
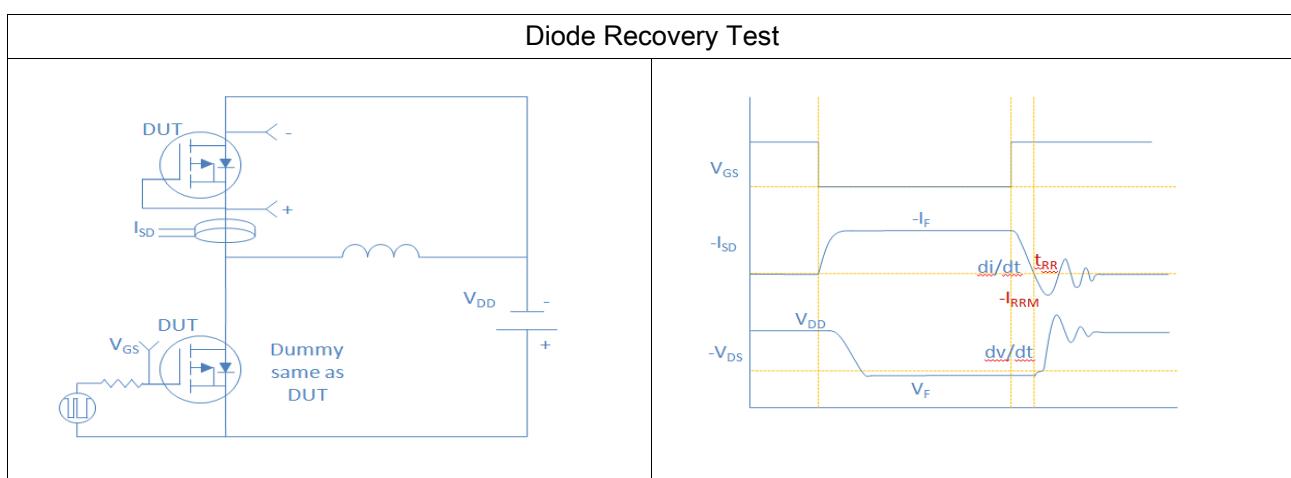
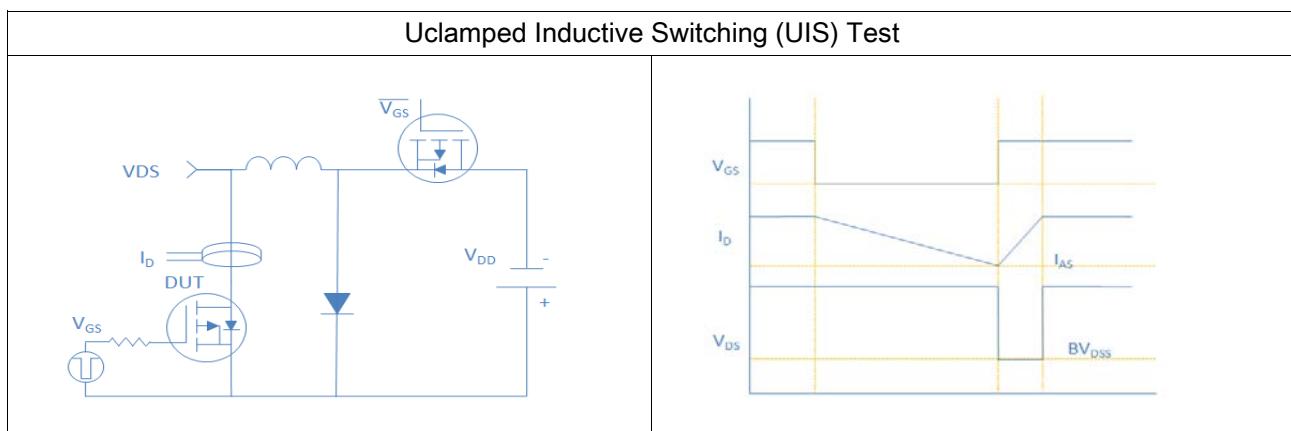
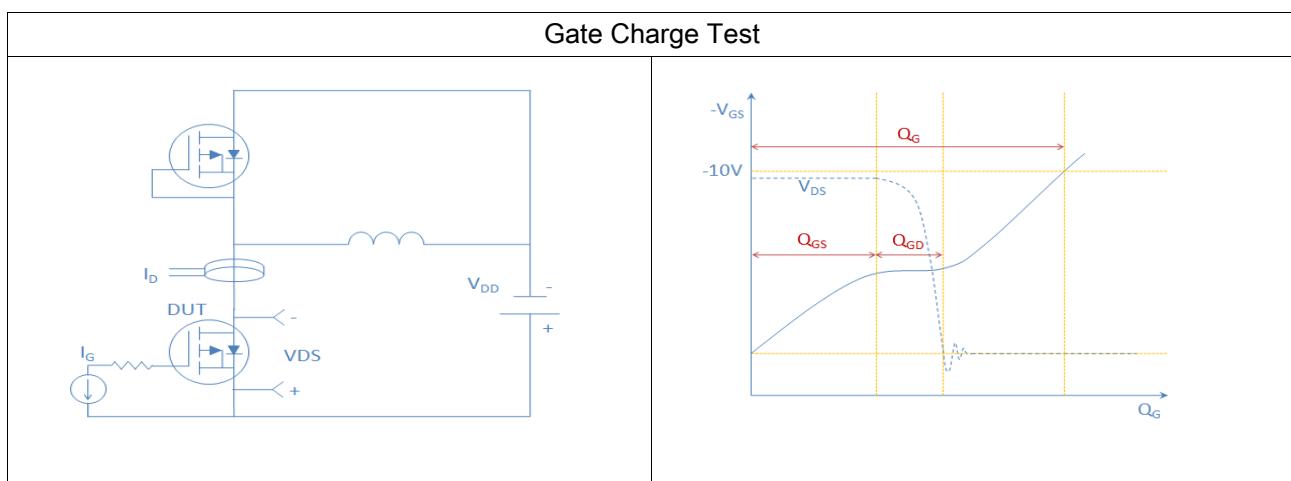
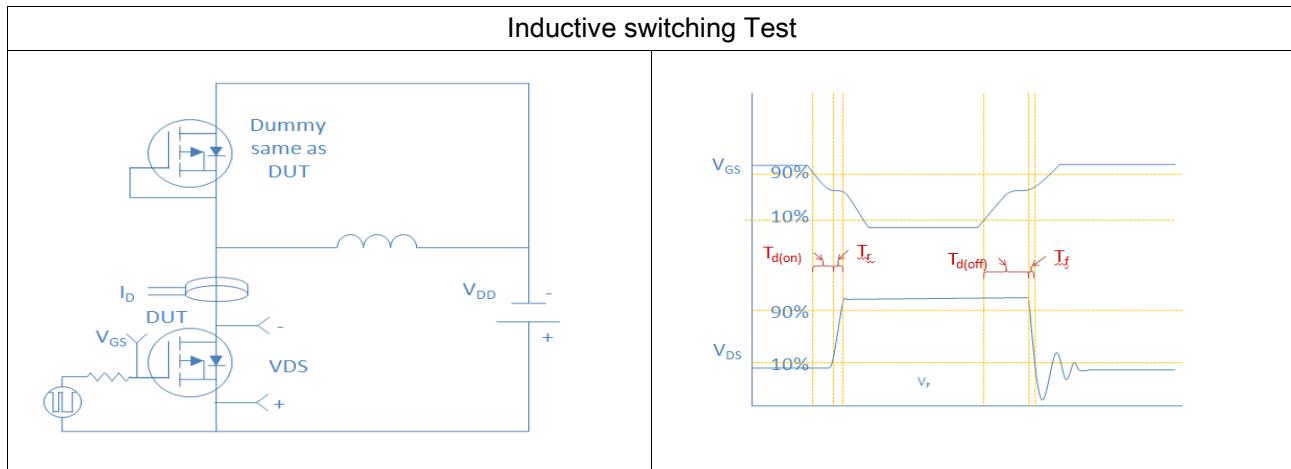


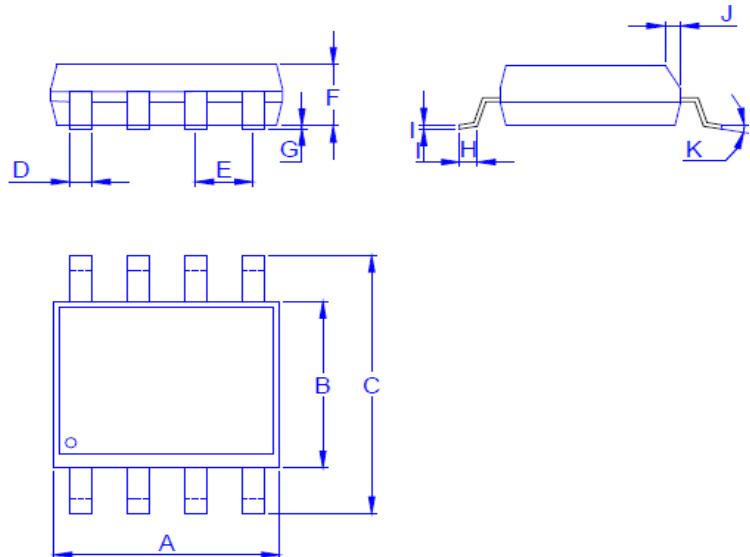
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Package Outline

SOIC-8, 8leads



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°